AMENDMENTS

In the Claims:

Please amend the claims as indicated hereafter.

1. (Previously Presented) An apparatus for performing addition of propagate, kill, and generate recoded numbers, said apparatus comprising:

circuitry configured to receive at least a first operand, a second operand, and a carry-in bit, the first and second operands comprising respective first and second propagate, kill, and generate recoded number representations of respective first and second binary operands;

a first carry-save adder configured to add said first operand and said second operand to generate a third propagate, kill, and generate recoded number representation and a carry-out bit; and

a modified carry-save adder configured to receive the third propagate, kill, and generate recoded number representation from the first carry-save adder and the carry-in bit from the circuitry, add the separate propagate, kill, and generate bits of the third propagate, kill, and generate recoded number representation with the carry-in bit to generate a sum value and a carry value, wherein the circuitry provides the carry-out bit from the first carry-save adder at a first output and the carry value from the modified carry-save adder at a second output,

wherein each of the propagate, kill, and generate recoded number representations has a respective kill bit, a respective propagate bit, and a respective generate bit that are indicative of a respective coded logical value having a plurality of bits, wherein the kill bit, if set, indicates that each of the bits of the respective coded logical value is not set, wherein the propagate bit, if set, indicates that only one of the bits of the respective coded logical value is set, and wherein the generate bit, if set, indicates that each of the bits of the respective coded logical value is set.

2. (Original) The apparatus of claim 1, wherein said sum value and said carry value are dual rail encoded values.

3-6. (Canceled)

7. (Previously Presented) A method for processing propagate, kill, and generate representations of respective first and second binary operands, comprising:

receiving a carry-in value and a first and a second propagate, kill, and generate representation of respective first and second binary operands;

generating a third propagate, kill, and generate representation and a carry-out value responsive to the first and second propagate, kill, and generate representations;

logically combining the third propagate, kill, and generate representation with the carry-in value to generate a sum value and a carry value; and

providing the carry-out value, the carry value, and the sum value as a result of the addition of the first and second propagate, kill, and generate representations,

wherein each of the propagate, kill, and generate recoded number representations has a respective kill bit, a respective propagate bit, and a respective generate bit that are indicative of a respective coded logical value having a plurality of bits, wherein the kill bit, if set, indicates that each of the bits of the respective coded logical value is not set, wherein the propagate bit, if set, indicates that only one of the bits of the respective coded logical value is set, and wherein the generate bit, if set, indicates that each of the bits of the respective coded logical value is set.

8. (Previously Presented) The method of claim 7, wherein said step of logically combining comprises adding the third propagate, kill, and generate representation and the carry-in value.

9. (Canceled)

10. (Previously Presented) The method of claim 7, wherein said step of logically combining further comprises generating dual rail encoded values.

11-22. (Canceled)

23. (Currently Amended) The apparatus of claim 1, wherein the sum value is a function of the ~~third~~ propagate bit of the third propagate, kill, and generate recoded number representation and the carry-in value.

24. (Currently Amended) The apparatus of claim 23, wherein the sum value is the XOR combination of the ~~third~~ propagate bit of the third propagate, kill, and generate recoded number representation and the carry-in value.

25. (Currently Amended) The apparatus of claim 1, wherein the carry value is a function of the ~~third~~ propagate bit of the third propagate, kill, and generate recoded number representation, the

carry-in value, and the ~~third~~ generate bit of the third propagate, kill, and generate recoded number representation.

26. (Currently Amended) The apparatus of claim 25, wherein the carry value is the OR combination of the ~~third~~ generate bit of the third propagate, kill, and generate recoded number representation with the AND combination of the ~~third~~ propagate bit of the third propagate, kill, and generate recoded number representation and the carry-in value.

27. (Currently Amended) The apparatus of claim 1, wherein the carry-out value is a function of the generate bit of the first propagate, kill, and generate recoded number representation and the generate bit of the second propagate, kill, and generate recoded number representation ~~generate representations~~.

28. (Currently Amended) The apparatus of claim 27, wherein the carry-out value is the OR combination of the generate bit of the first propagate, kill, and generate recoded number representation and the generate bit of the second propagate, kill, and generate recoded number representation ~~generate representations~~.

29. (Previously Presented) The apparatus of claim 1, wherein the circuitry provides the sum value at a third output.

30. (Currently Amended) The method of claim 7, wherein said step of logically combining comprises a XOR combination of the ~~third~~ propagate bit of the third propagate, kill, and generate recoded number representation and the carry-in value.

31. (Currently Amended) The method of claim 7, wherein said step of logically combining comprises an OR combination of the ~~third~~ generate bit of the third propagate, kill, and generate recoded number representation with the AND combination of the ~~third~~ propagate bit of the third propagate, kill, and generate recoded number representation and the carry-in value.

32. (Currently Amended) The method of claim 7, wherein said step of generating comprises an OR combination of the generate bit of the first propagate, kill, and generate recoded number representation and the generate bit of the second propagate, kill, and generate recoded number representation ~~generate representations~~.

33. (Previously Presented) The apparatus of claim 1, wherein only a respective one of the kill, propagate, and generate bits of each possible propagate, kill, and generate recoded number representation can be set.

34. (Previously Presented) The apparatus of claim 1, wherein each set bit of the logical value has a binary value of one.

35. (Currently Amended) An apparatus for performing addition, said apparatus comprising:

a first carry save adder configured to receive a first operand defining a first logical value encoded in propagate, kill, and generate (PKG) form such that the operand has a propagate bit, a generate bit, and a kill bit, the first carry save adder configured to receive a second operand defining a second logical value encoded in PKG form such that the second operand has a propagate bit, a generate bit, and a kill bit, the first carry save adder further configured to sum the first and second operands in PKG form to provide a first sum output in PKG form and a first carry bit without decoding the first and second operands from PKG form, the first sum output having a propagate bit, a generate bit, and a kill bit,

wherein the first carry bit and the propagate, generate, and kill bits of the first sum output collectively represent a summation of the first and second operands, wherein the first sum output represents a third logical value encoded in PKG form and equal to a sum of the first and second logical values, wherein the first logical value has a plurality of bits, wherein the kill bit of the first operand, if set, indicates that none of the bits of the first logical value are set, wherein the propagate bit of the first operand, if set, indicates that only one of the bits of the first logical value is set, and wherein the generate bit of the first logical value, if set, indicates that each of the bits of the first logical value is set, wherein the second logical value has a plurality of bits, wherein the kill bit of the second operand, if set, indicates that none of the bits of the second logical value are set, wherein the propagate bit of the second operand, if set, indicates that only one of the bits of the second logical value is set, and wherein the generate bit of the second logical value, if set, indicates that each of the bits of the second logical value is set, wherein the third logical value has a plurality of

bits, wherein the kill bit of the first sum output, if set, indicates that none of the bits of the third logical value are set, wherein the propagate bit of the first sum output, if set, indicates that only one of the bits of the third logical value is set, and wherein the generate bit of the first sum output, if set, indicates that each of the bits of the third logical value is set.

36. (Canceled)

37. (Previously Presented) The method of claim 7, wherein each set bit of the logical value has a binary value of one.

38. (Previously Presented) The method of claim 7, wherein only a respective one of the kill, propagate, and generate bits of each possible propagate, kill, and generate recoded number representation is set.

39. (Currently Amended) The apparatus of claim 35, wherein the first carry save adder is configured to set only a respective ~~a single~~ one of the kill, propagate, and generate bits of the first sum output ~~is set by the circuitry~~ regardless of the logical values defined by the operands.

40. (Currently Amended) The apparatus of claim 35, further comprising a second carry save adder configured to receive a second carry bit and the first sum output of the first carry save adder, the second carry save adder configured to sum the first sum output and the second carry bit to provide a second sum output having a third carry bit and a sum bit.

41. (New) The apparatus of claim 40, wherein the third carry bit is the OR combination of the generate bit of the first sum output with the AND combination of the propagate bit of the first sum output and the second carry bit.

42. (New) The apparatus of claim 1, wherein the first carry save adder is configured to set only a respective one of the propagate, kill and generate bits of the third propagate, kill, and generate recoded number representation for each possible state of the first and second propagate, kill, and generate recoded number representations.